UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,980	10/20/2003	Joseph Smart	2867-206	3802

27820 7590 05/12/2005

WITHROW & TERRANOVA, P.L.L.C.
P.O. BOX 1287
CARY, NC 27512

EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/689,980	SMART ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14 - 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14 - 29* is/are rejected.

7)☒ Claim(s) *27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim **27** is objected to because of the following informalities: Change "second region" t0 – gate region --. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims**14 – 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaska et al. (US Patent Application Publication no. 2004/0070003) in view of Beaumont et al. (US Patent no. 6,802,902).

4. Regarding claims **14** and **15**, Gaska shows a method of growing a gallium nitride epitaxial structure comprising:

Depositing a structural epitaxial 14/16 (fig. 2) including a GaN buffer layer [0029], [0030], [0031] and [0032);

Depositing a silicon nitride passivation layer on the GaN structural epitaxial layers.

Gaska does not explicitly discover a silicon nitride being under thermally activated deposition process before the GaN epitaxial structure is removed from an associated growth chamber.

However, Beaumont shows depositing a thermally assisted silicon layer 3 (fig. 1) on the structure epitaxial layers before the GaN epitaxial structure is removed from an associated growth chamber (col. 2, lines 35 – 37; col. 5, lines 54 and 55; note: the silicon nitride film being deposited in the growth chamber at 1080^0 C. using a thermally activated deposition process, (col. 8, lines 38 – 42), therefore, it has a characteristic of thermally assisted silicon nitride as claimed invention).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the silicon nitride layer using undefined process of Gaska with the silicon nitride using thermally process for depositing the silicon nitride layer in an associated growth chamber, in order to control the geometry and dispersion not being a perquisite for improving quality of the GaN layers (col. 9, lines 35 – 40).

Regarding **16**, Beaumont shows the depositing the passiivation layer step is a thermally activated deposition process (note: the silicon nitride film being deposited in the growth chamber at 1080^0 C. using a thermally activated deposition process, (col. 8, lines 38 – 42),

Regarding claims **17** and **18**, Gaska et al. disclose the depositing of structural epitaxial layers step comprising depositing a transitional layer 20 (fig. 3) on the substrate and a GaN buffer layer 22 (fig. 3) on the transitional layer (fig. 3; [0032]).

Regarding claim **19**, Gaska et al. show depositing an AlGaN Schottky layer 14 (fig. 3) on the GaN buffer layer ([0029] and [0032]).

Regarding claim **20**, Gaska et al. show depositing a GaN layer 16 (fig. 3; [0029]) on the AlGaN Schottky layer 14 (fig. 3)

Regarding claims **21** and **22**, Gaska et al. show the claimed invention of claims 14 and 17 except for step of depositing an AlN sub-buffer layer on the transitional layer as cited in claim 21 and depositing the GaN buffer layer on the sub-buffer layer.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to duplicate buffer layer 22 (note: layer can be any combination of AlN, GaN) with a sub-buffer layer made of AlN, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art

Regarding claim **23**, Gaska et al. show depositing an AlGaN layer 14 (fig. 3) on the GaN layer 22.

Regarding claim **24**, Gaska et al. show depositing a GaN layer 16 (fig. 3; [0029]) on the AlGaN Schottky layer 14 (fig. 3).

5. Claims **25 – 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaska et al. (US Patent Application Publication no. 2004/0070003) in view of Beaumont et al. (US Patent no. 6,802,902) and further in view of Nakano et al. (US Patent no. 5,698,870).

Regarding claim **25**, Gaska et al. show the claimed invention of claim 14 and source, gate, and drain regions of the passive layer (fig. 8) being etched for forming source contact 32 (fig. 8), gate 36A, and drain 34 (figs. 9 & 10) as cited in present claim.

Gaska and Beaumont do not explicitly show a step of etching the passivation layer and forming source, gate and drain contacts, thereby forming a high electron mobility transistor.

However, at the time the invention was made, It would have been an obvious to one having ordinary skill in the art to etch a source, gate, and drain regions as shown by Nakano for a HEMT (col. 18, lines 17 – 25). Applicant has not disclosed etching the passivation layer to form source, gate and drain contacts provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either etching method or undisclosed method because both methods introduce the source, drain and gate regions.

Therefore, it would have been obvious to ordinary skill in this art to use etching method to obtain the invention as specified in claim 25.

Regarding claim **26**, Nakano shows the source, drain and gate regions of silicon nitride layer are etched using wet chemical etching (col. 18, lines 17 – 25).

Regarding claim **27**, Gaska, Beaumont and Nakano disclose the claimed invention of claims 14 and 25 except for using dry chemical etch to form gate region.

However, at the time the invention was made, It would have been an obvious to one having ordinary skill in the art to use wet chemical etch for forming a source, gate, and drain regions as shown by Nakano for a HEMT (col. 18, lines 17 – 25). Applicant has not disclosed dry chemical etching the passivation layer to form a gate region provides an advantage, is used for a particular purpose, or solves a stated problem.

One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either dry chemical etching method or wet chemical etching method because both methods introduce the region.

Therefore, it would have been obvious to ordinary skill in this art to use etching method to obtain the invention as specified in claim 27.

Regarding claim **28**, Gaska et al. show the claimed invention of claim 14 and: source and drain regions of the passive layer being etched for forming source contact 32B (fig. 9), gate 36B, and drain 34B (fig. 9) as cited in present claim.

Gaska and Beaumont do not explicitly show a step of etching the passivation layer and forming source, gate and drain contacts.

However, at the time the invention was made, It would have been an obvious to one having ordinary skill in the art to use wet chemical etch to form a source and drain regions as shown by Nakano (col. 18, lines 17 – 25). Applicant has not disclosed etching the passivation layer to form source and drain contacts provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either etching method or undisclosed method because both methods introduce the source and drain regions.

Therefore, it would have been obvious to ordinary skill in this art to use etching method to obtain the invention as specified in claim 28.

In addition, Gaska, Beaumont and Nakano do not the device is a metal-insulator-semiconductor field effect transistor. However, the device of Gaska, Beaumont and

Nakano ar similar to that of the claimed invention, therefore, it is fair to say it is a metal-insulator-semiconductor field effect transistor as claimed.

Regarding claim **29**, Nakano shows the drain and source regions of the silicon nitride layer are etched using a wet chemical etch.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran LKT

May 6, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800